REMARKS/ARGUMENTS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

The examiner has rejected claims 1-5, and 11-14.

Additionally, Examiner has rejected and withdrawn claims 5-10 as being drawn to a non-elected invention.

By way of the foregoing amendments, claims 1, 6, and 11 have been amended.

Claims 2, 5, 8, and 12 have been cancelled without prejudice.

Claims 1, 3, 4, 6, 7, 9, 10, 11, 13, and 14 have been amended.

Claims 15-18 are newly added.

Accordingly, upon entry of this Response, Claims 1, 3, 4, 6, 7, 9, 10, 11, 13-18 are pending.

The changes in the claims do not introduce new matter but clarify matters shown and described in the application as filed. The foregoing amendments and following remarks are believed to be fully responsive to the Office Action mailed August 12, 2003 and render all currently pending claims at issue patentably distinct over the references cited by the Examiner.

The foregoing amendments are taken in the interest of expediting prosecution and there is no intention of surrendering any range of equivalents to which Applicant would otherwise be entitled in view of the prior art. Reconsideration and examination of this application is respectfully requested in light of the foregoing amendments and the following remarks.

EXAMINER'S OFFICE ACTION

In the August 12, 2003 Office Action referenced above, the Examiner:

rejected and withdrew claims 6-10 as being drawn to a non-elected invention;

rejected Claims 1, 3, 5, 11, and 13 under 35 USC § 102(b) as being anticipated by Strodbeck, U.S. Patent No. 6,150,838 (hereinafter "STRODBECK");

rejected Claims 1 and 3 under 35 USC §102(b) as being as being anticipated by DAISUKE MATSUNAGA, Japanese Publication No. JP 05129421 (hereinafter "MATSUNAGA"); and

rejected Claims 2, 4, 12, and 14 under 35 USC §103(a) as being obvious over STRODBECK in view of Kiyoaki Kumazaki, Japanese Patent No. 11214484 (hereinafter "KUMAZAKI").

Rejection Of Claims Drawn To Non-Elected Invention

Claims 6-10 are rejected as being drawn to a non-elected invention. In August 12, 2003 office action, the Examiner withdrew claims 6-10. Accordingly, independent claim 6 has been amended to define a method in accordance with the elected invention of claim 11.

The rejection of Claims 6-10 based on claims 6-10 being drawn to a non-elected invention is respectfully traversed.

Claim 6 has been amended to patentably define subject matter directed to the invention as claimed in elected claim 11.

With regard to amended claim 6, the terminology "detecting an out of position wafer in a microchip fabrication chamber as claimed in" has been deleted and the terminology a method of "using the microchip fabrication apparatus of claim 11 has been added to further define the step of using the apparatus as defined in amended apparatus claim 11. Thus, like claim 11, claim 6 is directed to a method of using a microchip fabrication apparatus having a "tip of at least one of said plurality of lift mechanism pins having capacitive

proximity sensing means disposed substantially within the tip for detecting the proximity of the wafer."

Thus, claim 6 is now directed to a method of using the same elected invention as is claimed in elected and amended claim 11.

Additionally, Claims 7-10 which depend from claim 6 are now considered to be directed to the elected invention.

In light of amendments to Claim 6, Examiner's rejections based on claims drawn to a non-elected invention have been obviated.

Claim Rejections Under 35 USC § 102(b)

Claims 1, 3, 5, 11, and 13 are rejected under 35 USC § 102(b) as being anticipated by STRODBECK.

Additionally Claims 1 and 3 are rejected under 35 USC §102(b) as being as being anticipated MATSUNAGA.

The rejection of claims 1, 3, 5, 11, and 13 under 35 USC § 102(b) based on STRODBECK and MATSUNAGA is respectfully traversed.

STRODBECK teaches a thermal conditioning apparatus 10 that operates to exhaust vapors emanating from a surface, thermal conditioning apparatus 10 having a thermal conditioning plate 12 having at least three lift pin holes 56 for receiving support pins 60. See STRODBECK, ABSTRACT, col. 5, lines 19-20, 41-46, and col. 6, lines 12-15. "The support pins 60 have bores therethrough which provide fluid communication between the proximal ends 62 of the support pins 60 and the vacuum port 58, thereby allowing a vacuum to be drawn through the support pins 60." STRODBECK, Col. 6, lines 15-19.

Additionally, STRODBECK provides that a vacuum sensor can be attached to a computer controller 16 to determine the

presence of a wafer 19 on the support pins 60. See STRODBECK, col. 6, lines 46-50.

In an alternative embodiment, STRODBECK provides three elongated cylindrical lift pins 70 each having a longitudinal bore extending from a contacting end 72 for holding an infared wafer sensor 74 at distance apart from the contacting end 72 of the lift pin 70. Col. 6, lines 51-55. **"The lift pin bore is preferably counter sunk or dish machined out at the contacting end 72 to allow the sensor beam to fan out and the sensor 74 to be placed farther away from the contacting end 72 so as to minimize damage to the sensor 74 and the wafer 19."** STRODBECK, Col. 6, lines 63 through Col. 7, line 1.

STRODBECK further teaches use of a vacuum or mechanical sensor used to detect presence of a wafer. "Different types of sensors, such as vacuum or mechanical sensors, can also be employed within the scope of the invention. STRODBECK, Col. 7, lines 4-6. "[I]f the lift pins 70 are constructed with a central bore, a vacuum can be applied directly to the lift pins 70." STRODBECK, Col. 7, lines 14-16.

The MATSUNAGA reference teaches a wafer retaining stand 1 retaining wafer, lift pins 3 moving the wafer vertically on the wafer retaining stand 1, and stress sensors 4 disposed at a predetermined distance below a tip of the lift pins 3 for detecting stress applied to the lift pins at the time of vertical movement. See MATSUNAGA, ABSTRACT, and FIG. 1-7. The stress sensors 4 are depressed when a wafer is placed on the lift pins and signal an output from the stress sensor to a CPU. Additionally, the stress sensors are preferably, a spring, a piezoelectric element, or a pressure gauge.

The present invention discloses a microchip fabrication apparatus for processing a wafer having:

a chamber for processing the wafer;

a plurality of lift mechanism pins (21-23) within the chamber for supporting the wafer 30; and

a plurality of **capacitive proximity** sensors 55 **disposed substantially at a tip 57 of each of said plurality of lift mechanism pins** 21-23 for detecting the wafer position.

Support for amending claim 1, and 11 to include the features of **capacitive proximity** sensors **disposed substantially at a tip of each of said plurality of lift mechanism pins** is found in Pending Application, FIGS. 4-5, and ¶ 0031-0032.

> "Rather than the exemplary **capacitive proximity sensing** as previously described with respect to individual pin sensing the circuitry of Fig. 6 senses capacitance between pairs of pins. Each pin in a four pin lift mechanism is provided with a probe electrode 61, 63, 65, 67 substantially at each respective tip."

Pending Application, ¶ 0031.

"Figs. 4 and 5 illustrate one exemplary embodiment of a pin arrangement adapted for capacitive sensing wherein each pin 50 **has a central longitudinal bore 53 through which a probe electrode 55 is disposed. An insulative layer 59 is located between the central electrode 55 and the outer core 51 of the pin 50 if the pin is itself conductive. Electrode 55 is exposed at the tip 57 of pin 50 such that it is proximate the underside or bottom of the wafer and preferably in contact therewith when the wafer is carried by the pin 50.**" Pending Application, FIGS. 4-5, and ¶ 0032.

Claims 2, 5, 8, and 12 have been cancelled without prejudice.

With regard to claims 2 and 12, the limitations of dependent Claims 2 and 12 have been incorporated into claims 1 and 12, respectively.

With regard to claims 3, 4, 13, and 14 claims 3, 4, 13, and 14 have been amended to further define the features of the capacitive proximity sensing means.

The STRODBECK references teaches away from the capacitive sensing means disposed within the tip of the lift pins of the present invention. Instead, STRODBECK provides a longitudinal bore and an infa-red sensor placed **away from the tip** of the lift pin. The bore is counter-sunk to allow for the beam to spread out. Additionally, the actual infa-red sensor is placed away from the bore to avoid contact with the wafer.

The structural limitations taught in the STRODBECK reference are different than the structural limitations of the present invention. Unlike STRODBECK, the present invention does not require that the lift pin bore be countersunk. Instead, the lift pin bore 53 of the present invention extends in a uniform manner from the tip 57 of the pin 50 contacting the wafer and accommodates a probe electrode 55 therewithin, wherein the probe electrode 55 extends from the tip of the pin 57 through the length of the bore 53. See Present Application, FIGS. 4-5.

Additionally, unlike the STRODBECK invention, the present invention teaches that the probe electrode 55 (a capacitive sensor) be placed at the tip 57 of the lift pin 50 to actually contact the wafer. As discussed, **supra**, the infa-red sensor of STRODBECK is placed away from the tip of the support pins 60, 70 to avoid contact and damage to a wafer 19.

While STRODBECK does teach use of a mechanical or vacuum sensor, nowhere does STRODBECK disclose, teach, or suggest that the mechanical or vacuum sensor contact the wafer and be

placed at the tip of the support pins 60, 70. Additionally, the teaching of a vacuum sensor of STRODBECK is contrary to the teaching of the present invention. The present invention places an electric probe throughout the length of the bore to sense presence of a wafer by contacting the wafer. However, the vacuum sensor requires that the bore be **HOLLOW** in order to form a vacuum within the bore. If there was a probe electrode sensor placed within the bore of the STRODBECK invention, the path to the vacuum pump would be blocked and thus, a vacuum could not be formed within the bore.

The STRODBECK additionally does not disclose, teach or suggest that a capacitive sensor be used in combination with a mechanical sensor. Therefore,STRODBECK, teaches away from a lift pin having a bore extending therethrough, the bore having an electric probe disposed within bore to contact a wafer of the present invention at a tip of the lift pin.

Unlike the lift pins of the present invention, the lift pins 3 of the MATSUNAGA reference do not disclose capacitive sensing means disposed within the tips of the lift pins 3. As shown in MATSUNAGA, FIG. 1, the sensors 4 are placed at a predetermined distance away from the tip of the lift pin, and thus are not designed to actually contact a wafer.

Additionally, unlike the present invention, the MATSUNAGA reference fails to disclose a longitudinal bore disposed within the lift pin 3 to house a capacitive probe electrode sensor.

Additionally, neither the STRODBECK nor the MATSUNAGA references provide a means or a method for determining improper wafer positioning. The STRODBECK reference senses only if a wafer is present on conditioning plate 12 and does not provide means or a method to detect wafer position (misalignment or a broken wafer) disposed on the conditioning

plate 12. Similarly, the MATSUNAGA reference only senses whether a wafer is present on the wafer retaining stand 1 and does not determine actual wafer position on the wafer stand 1.

According to MPEP § 706.02, anticipation under 35 U.S.C. §102 requires that "the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." Here, the STRODBECK and the MATSUNAGA references fail. The references do not teach, suggest, or even remotely hint that the wafer position detection sensor be capacitive and be disposed in the tip of a lift pin. Thus, the present invention, as set forth in the now amended claims, is clearly distinct from the art of record.

Thus, the rejection of the claims 1, 3, 5, 11, and 13 under 35 USC § 102(b) have been obviated.

Claim Rejections Under 35 USC § 103(a)

Claims 2, 4, 12, and 14 are rejected under 35 USC §103(a) as being obvious over STRODBECK in view of KUMAZAKI.

The rejection of claims 2, 4, 12, and 14under 35 USC § 103(a) based on STRODBECK in view of KUMAZAKI is respectfully traversed.

Clearly, the device and methods disclosed in the STRODBECK reference does not anticipate the claimed invention. Thus, the STRODBECK references fails to disclose, teach, or suggest a using the claimed features of claims 1, 6, and 11, of the present invention from which claims 2, 4, 12, and 11 depend.

Applicant has amended independent claims 1, 6, and 11 and dependent claims 3, 4, 7, 9, 10, and 13-14 to further distinguish the present invention over the apparatuses disclosed in STRODBECK and KUMAZAKI references.

The KUMAZAKI teaches a substrate detector that detects a wafer disposed within a slot of a wafer cassette as the sensor approaches the wafer. The sensor 50 of the KUMAZAKI reference teaches a sensor that is adjacent to the wafer and does not necessarily contact the wafer.

The structure of the substrate detector having a capacitive sensor in the KUMAZAKI reference is different from the structure of the present invention. The sensor 50 of the KUMAZAKI reference teaches a sensor that is adjacent to the wafer and does not necessarily contact the wafer. Unlike the sensor taught in KUMAZAKI, the sensor of the present invention contacts and supports an underside of a wafer disposed upon the plurality of lift mechanism pins.

There is no motivation to combine the sensors disclosed in the STRODBECK reference with the capacitive sensor of the KUMAZAKI reference to get a capacitive sensor disposed within a tip of a lift pin to detect presence of a wafer. As mentioned supra, a capacitive sensor is neither taught nor suggested in the STRODBECK reference. The STRODBECK reference does teach using other sensors such as a vacuum sensor or a mechanical sensor. The teaching of a Vacuum sensor teaches away from a capacitive sensing means disposed within the bore because the vacuum sensor used in the STRODBACK reference uses an empty bore to form a vacuum inside of the hollow bore of the pin. Additionally, STRODBECK does not disclose use of the mechanical sensor with a capacitive sensor. Thus, the STRODBECK reference fails to teach or suggest a capacitive sensing means disposed within the tip of the bore.

As mentioned **supra**, the references of record disclosed herewithin do not disclose, teach, or suggest the features of independent Claims 1, 6, and 11, that define the apparatus and

steps of providing a microchip fabrication apparatus for processing a wafer having:

a plurality of **capacitive proximity** sensors **disposed substantially at a tip of each of said plurality of lift mechanism pins** for detecting the wafer position.

Thus, Claims 1, 6, and 11, are novel and non-obvious in light of the references of record cited herewithin. Additionally, the claims which depend from those claims are also novel and non-obvious in light of the references of record cited herewithin.

With regard to amended claim 6, as mentioned in the Rejection Of Claims Drawn To Non-Elected Invention section, **supra**, the terminology "detecting an out of position wafer in a microchip fabrication chamber as claimed in" has been deleted and the terminology a method of "using the microchip fabrication apparatus of claim 11 has been added to further define the step of using the apparatus as defined in amended apparatus claim 11. Thus, like claim 11, claim 6 is directed to a method of using a microchip fabrication apparatus having a "tip of at least one of said plurality of lift mechanism pins having capacitive proximity sensing means disposed substantially within the tip for detecting the proximity of the wafer."

Because claim 11 defines a novel and nonobvious apparatus, the method of using the apparatus of claim 11, as defined in claim 6 is also novel and nonobvious in light of the references of record cited herewithin.

With regard to claims 7, 9, and 10, which depend from claim 6, each claim has been amended to properly depend upon claim 6 by deleting the terminology "detecting an out of position wafer in a microchip fabrication chamber as claimed in".

With regard to claim 17, which depends upon claim 6 has been added to define the step of:
"determining if a wafer is out of position." Support for defining the step as claimed in newly added claim 17 is found Pending Application, ¶ 0031, 0034.

Unlike the present invention, none of the references cited herewithin disclose the step of determining if a wafer is out of position. The references of record cited herewithin operate to determine if a wafer is present but do not disclose, teach, or suggest a step of determining whether the wafer is out of position or is properly positioned.

With regard to claim 18, Claim 18 which depends from claim 17 has been added to define the step of: "providing a capacitive sense logic circuit in communication with the capacitive proximity sensor to perform the step of determining if a wafer is out of position." Like newly added claim 15, support for adding claim 18 to define the step of providing a capacitive sense logic circuit is found in Pending Application, ¶ 0031, 0033, and FIGS 6 and 9.

As mentioned supra, no such step of providing a capacitive sense logic circuit is disclosed in the references of record cited herewithin.

With regard to Claim 15, which depends from independent claim 1 has been added to define "a capacitive sense logic circuit in communication with the capacitive proximity sensor for determining if a wafer is out of position."

"The output lines 75 and 73 of capacitive sense circuits C1 70 and C2 71, respectively, provide a binary signal 0 to indicate that at least one of the pins of the respective pair of pins is not coupled to the bottom of a wafer and a 1 to indicate that both of the pins of the

respective pair of pins are commonly coupled to the bottom of a wafer." Pending Application, ¶ 0031.

Additional support for the capacitive sense logic circuit is found in Pending Application, ¶ 0033, and FIGS 6 and 9.

Unlike the present invention, no such capacitive sense logic circuit is disclosed in the references of record cited herewithin.

Claim 16, which depends from dependent claim 3, has been newly added to define the features of "the pairs of the plurality capacitive proximity sensors [used to] detect a capacitance between an associated pair of lift mechanism pins." Support for the newly added Claim 16 is found in Pending Application, ¶ 0031.

> "Rather than the exemplary capacitive proximity sensing as previously described with respect to individual pin sensing the circuitry of Fig. 6 **senses capacitance between pairs of pins**. Each pin in a four pin lift mechanism is provided with a probe electrode 61, 63, 65, 67 substantially at each respective tip. **Capacitance between pairs of electrodes 61,63 and 65,67 are detected by conventional capacitive sense circuits C1 70 and C2 71, respectively**. Experimental results have confirmed that a capacitance of substantially 0 picofarads between pairs of pins that are not commonly coupled to the bottom of a wafer results, whereas a capacitance of substantially 40 picofarads between pairs of pins that are commonly coupled to the bottom of a wafer results."

Pending Application, ¶ 0031.

Unlike the present invention, none of the references cited herewithin disclose having pairs of plurality capacitive proximity to detect the capacitance between two lift mechanism pins.

With regard to claim 14, claim 14, which depends from claim 11, has been amended to further define the probe

electrode, wherein **the probe electrode extends from a tip of the at least one of said plurality of lift mechanism pins through the central bore.**

The support for further defining the probe electrode is disclosed in the Pending Application, FIGS. 4-5, and ¶ 0032. None of the references of record disclosed herewithin define the features of the probe electrode of the present invention.

Thus, the present invention, as set forth in the now amended claims 1, 6, and 11, the claims which depend from claims 1, 6, and 11 respectively are clearly distinct from the art of record.

Based on the above, it is respectfully submitted that the amended claims 1, 3, 4, 6, 7, 9, 10, 11, 13-14 and newly added claims 15-18 are in condition for allowance, which allowance is earnestly solicited. With respect to the remaining claims, all of which depend from claims 1, 6, and 11, the fact that they claim additional elements or limitations also renders them allowable over STRODBECK, MATSUNAGA, and KIYOAKI KUMAZAKI which allowance is earnestly solicited.

It is believed that the present invention as amended is novel and nonobvious over the reference relied upon by the Examiner.

The rejection of claims 1-5, and 11-14 under 35 USC § 102(b) based on anticipation and under 35 USC § 103(a) based on obviousness is respectfully traversed. Additionally, rejection and withdrawal of claims 6-10 as amended as being directed to a non-elected invention is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

Based on the foregoing, the Applicant respectfully submits that all of the pending claims, i.e. claims 1, 3, 4, 6, 7, 9, 10, 11, and 13-18 are now in condition for allowance.

Such favorable action by the Examiner at an early date is respectfully solicited.

If for some reason Applicant has not requested a sufficient extension and/or have not paid a sufficient fee for this response and/or for the extension necessary to prevent the abandonment of this application, please consider this as a request for an extension for the required time period and/or authorization to charge our Deposit Account No. 50-0484 for any fee which may be due.

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicant's representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,
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